

When using this system, the user should refer to the user manual for the correct use of the system.

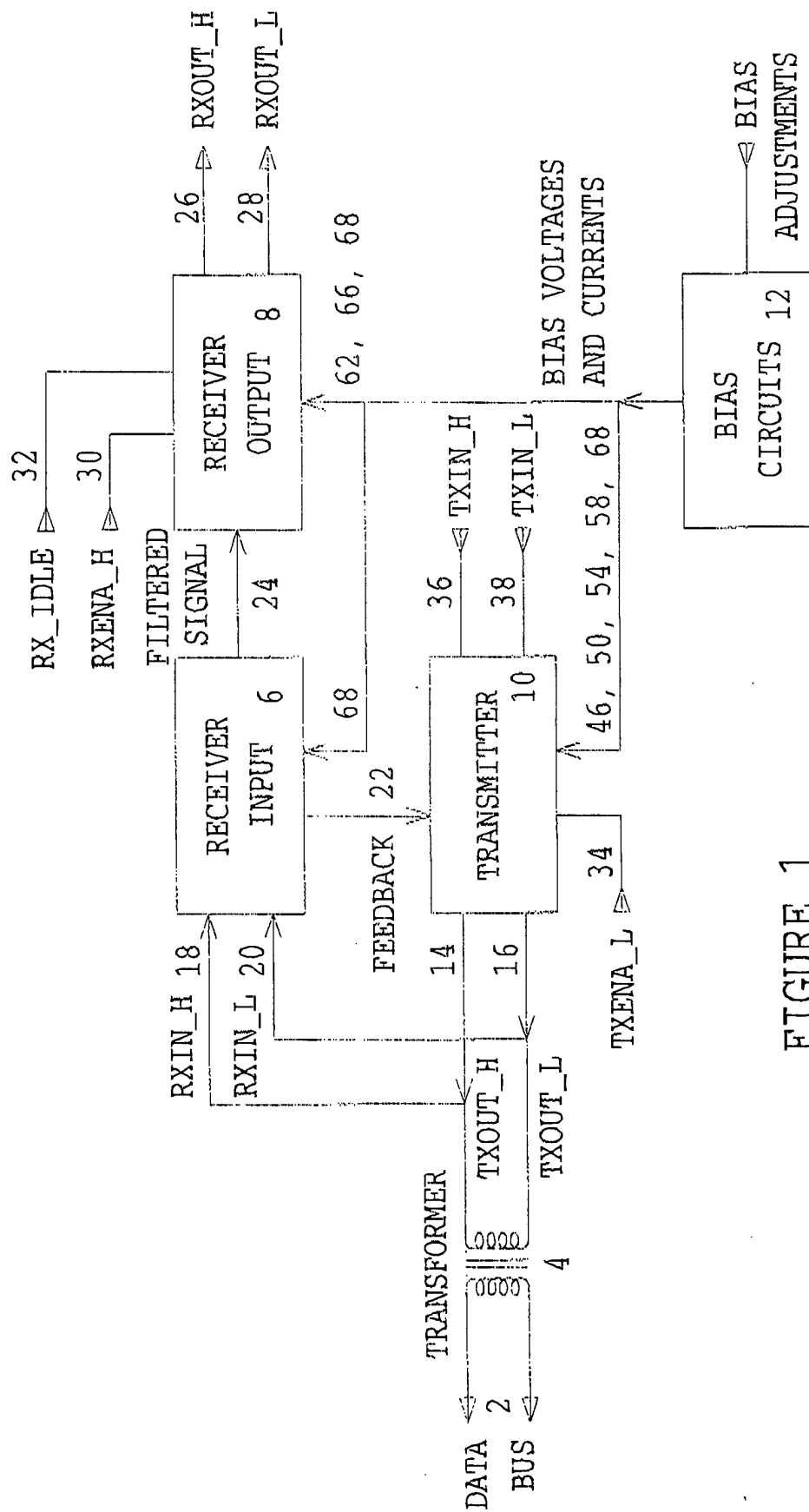


FIGURE 1

FIG. 2 is a schematic diagram of a differential amplifier circuit in accordance with the present invention. The circuit includes a first differential amplifier 200, a second differential amplifier 202, a third differential amplifier 204, and a fourth differential amplifier 206. The first differential amplifier 200 has a non-inverting input (+) connected to a feedback signal 22 and an inverting input (-) connected to a feedback signal 22. The second differential amplifier 202 has a non-inverting input (+) connected to a feedback signal 22 and an inverting input (-) connected to a feedback signal 22. The third differential amplifier 204 has a non-inverting input (+) connected to a feedback signal 22 and an inverting input (-) connected to a feedback signal 22. The fourth differential amplifier 206 has a non-inverting input (+) connected to a feedback signal 22 and an inverting input (-) connected to a feedback signal 22.

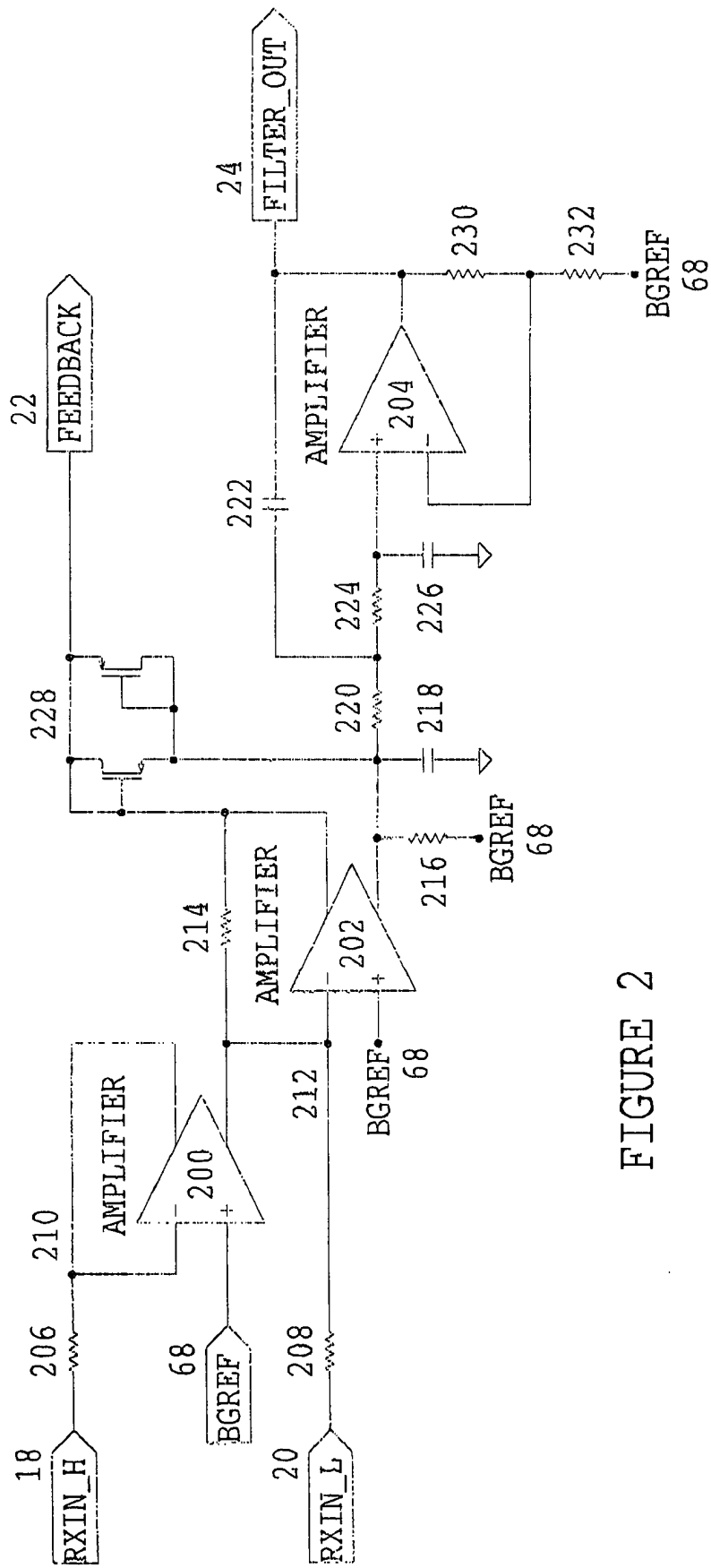


FIGURE 2

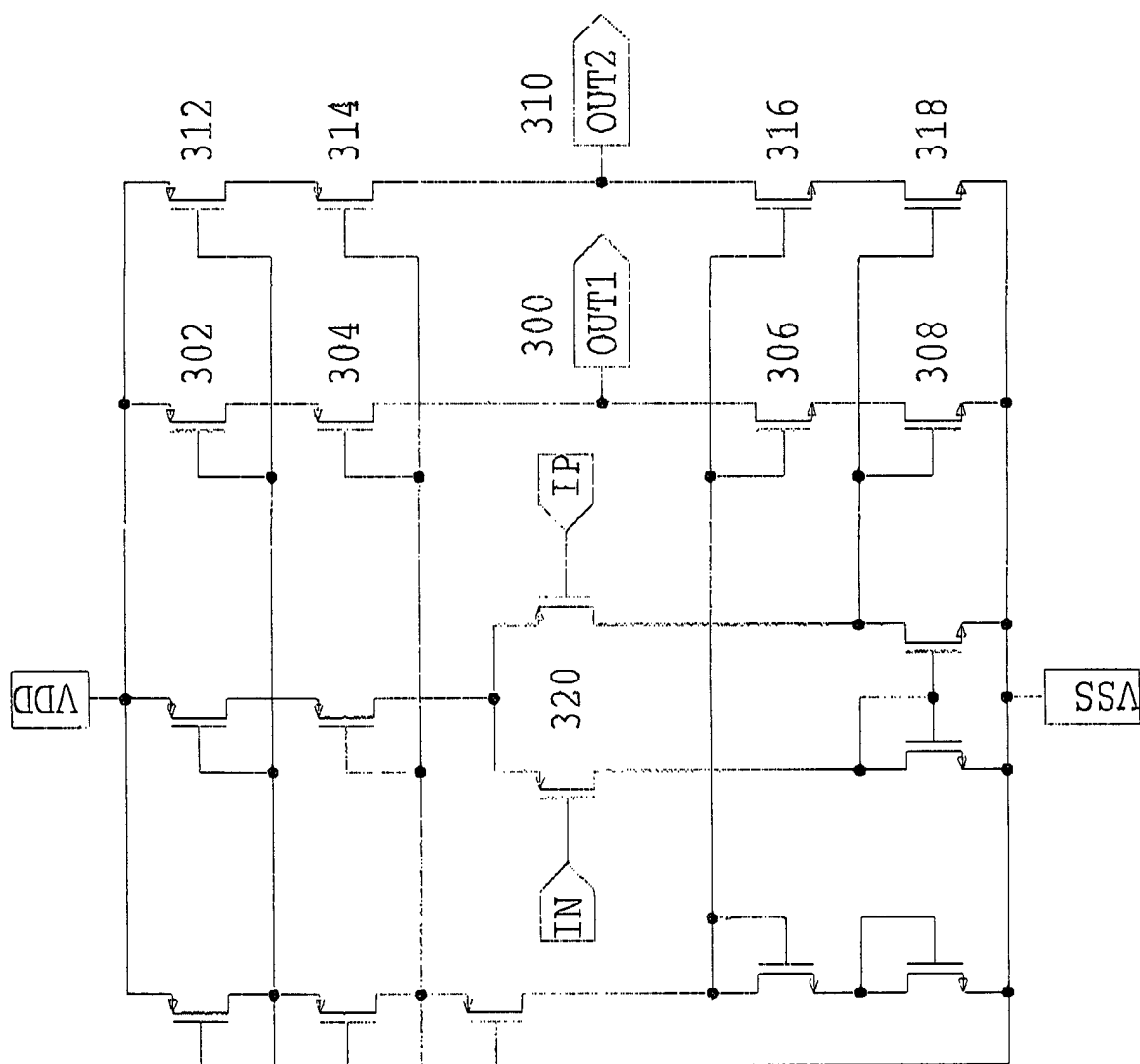


FIG. 4 is a block diagram of a receiver circuit 400 in accordance with one embodiment of the present invention. The receiver circuit 400 includes a first comparator 410 and a second comparator 414. The first comparator 410 has a non-inverting input (+) connected to a threshold voltage VTHP 66 and an inverting input (-) connected to a filter output FILTER_OUT 24. The second comparator 414 has a non-inverting input (+) connected to a threshold voltage VTHN 62 and an inverting input (-) connected to a background reference voltage BGRF 68. The output of the first comparator 410 is a signal NOT_BELOW 412, and the output of the second comparator 414 is a signal NOT_ABOVE 416. The receiver circuit 400 also includes a first AND gate 422, a second AND gate 424, a third AND gate 426, a fourth AND gate 428, a first OR gate 430, a second OR gate 432, a first ESD protection device ESD3 434, a second ESD protection device ESD3 436, a first output driver RXOUT_L 28, a second output driver RXOUT_H 26, a first enable input ENA_L 30, a second enable input RXENA_H 30, a first disable input DISABLE 32, and a first idle input RX_IDLE 32. The first AND gate 422 has inputs RX_LOW and ENA_H. The second AND gate 424 has inputs RX_HIGH and ENA_H. The third AND gate 426 has inputs BETWEEN and ENA_H. The fourth AND gate 428 has inputs DISABLE and ENA_L. The first OR gate 430 has inputs RX_LOW and ENA_H. The second OR gate 432 has inputs RX_HIGH and ENA_H. The first ESD protection device ESD3 434 is connected to the output of the first OR gate 430 and the first output driver RXOUT_L 28. The second ESD protection device ESD3 436 is connected to the output of the second OR gate 432 and the second output driver RXOUT_H 26. The first enable input ENA_L 30 is connected to the first AND gate 428 and the first OR gate 430. The second enable input RXENA_H 30 is connected to the first AND gate 422 and the second OR gate 432. The first disable input DISABLE 32 is connected to the first AND gate 428 and the first OR gate 430. The first idle input RX_IDLE 32 is connected to the first AND gate 422 and the second OR gate 432.

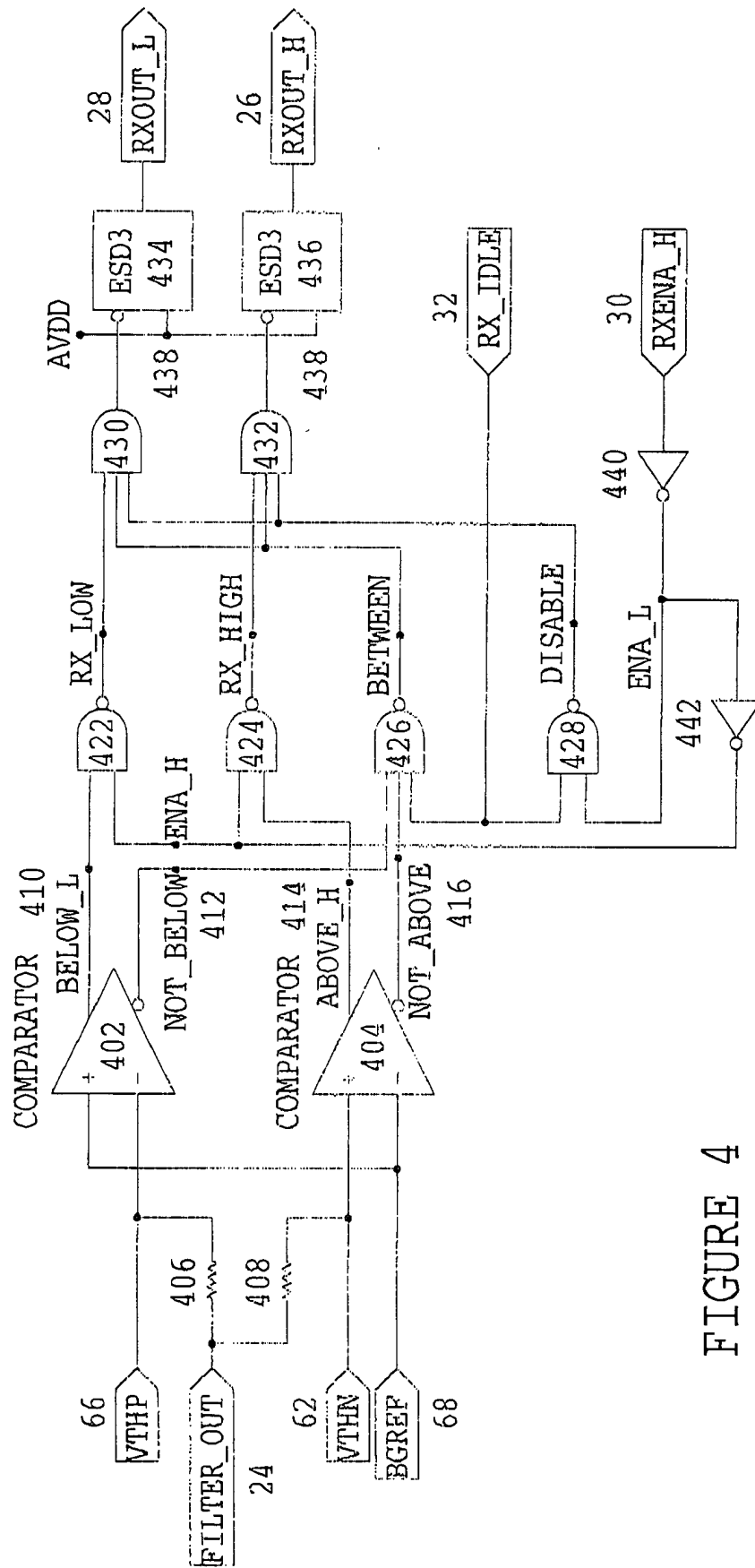


FIGURE 4

FIG. 5 is a schematic diagram of a circuit in accordance with the present invention.

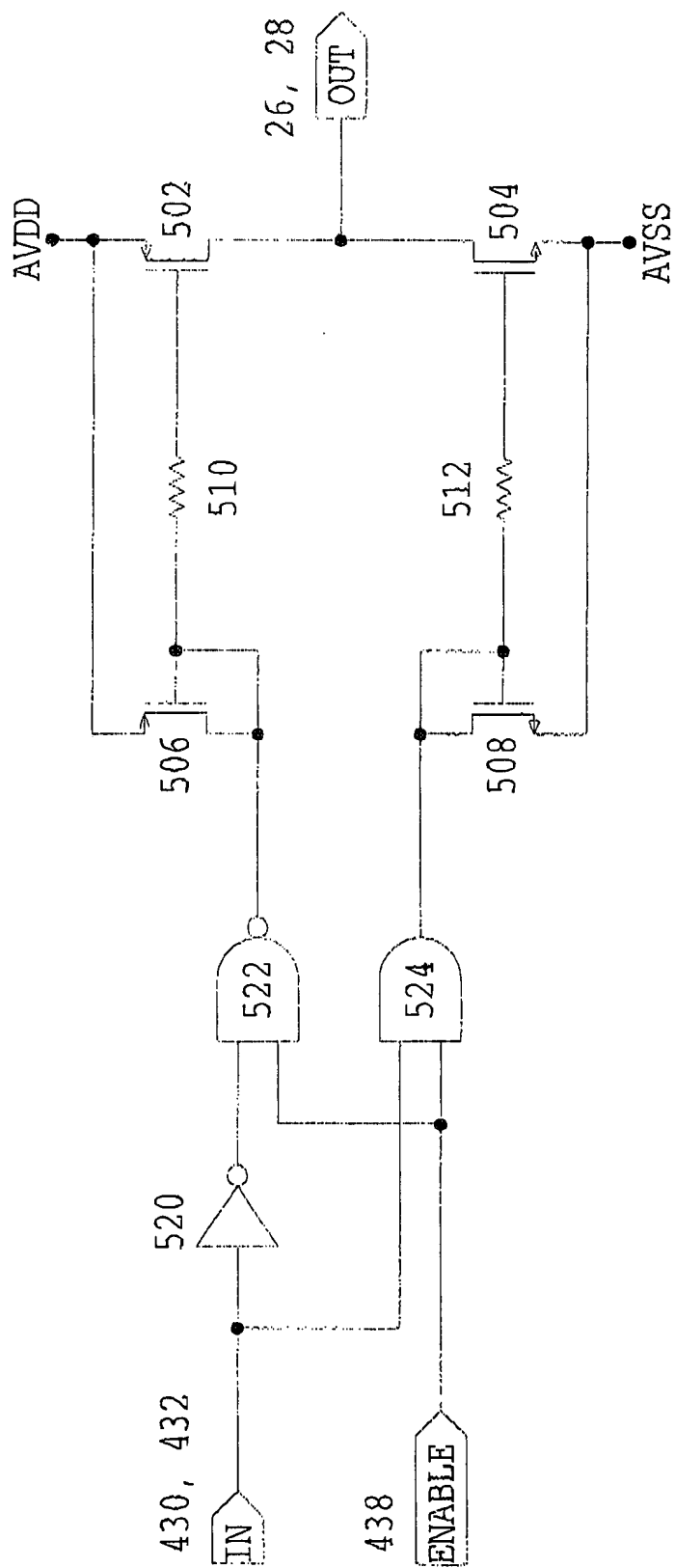


FIGURE 5

FIG. 6 is a schematic diagram of a transmitter circuit in accordance with the present invention. The circuit includes a TXIN_H input (36), a TXIN_L input (38), and a TXENA_L enable input (34). The TXIN_H and TXIN_L inputs are connected to inverters 610 and 612, respectively. The outputs of inverters 610 and 612 are connected to NAND gates 600 and 602, respectively. The TXENA_L input is connected to the output of NAND gate 602. The outputs of NAND gates 600 and 602 are connected to TX_HIGH and TX_LOW signals, respectively. These signals are then connected to a transmitter block (dashed box) which includes inverters 614 and 616, and transistors 700, 702, 704, and 706. The TX_HIGH signal is connected to the gate of transistor 700, which is connected to TXOUT_H (14). The TX_LOW signal is connected to the gate of transistor 702, which is connected to TXOUT_L (16). The TXOUT_H and TXOUT_L signals are connected to the gates of transistors 704 and 706, respectively. The gates of transistors 704 and 706 are also connected to the gates of transistors 700 and 702, respectively. The sources of transistors 700 and 702 are connected to AVDD and AVSS, respectively. The sources of transistors 704 and 706 are connected to AVDD and AVSS, respectively.

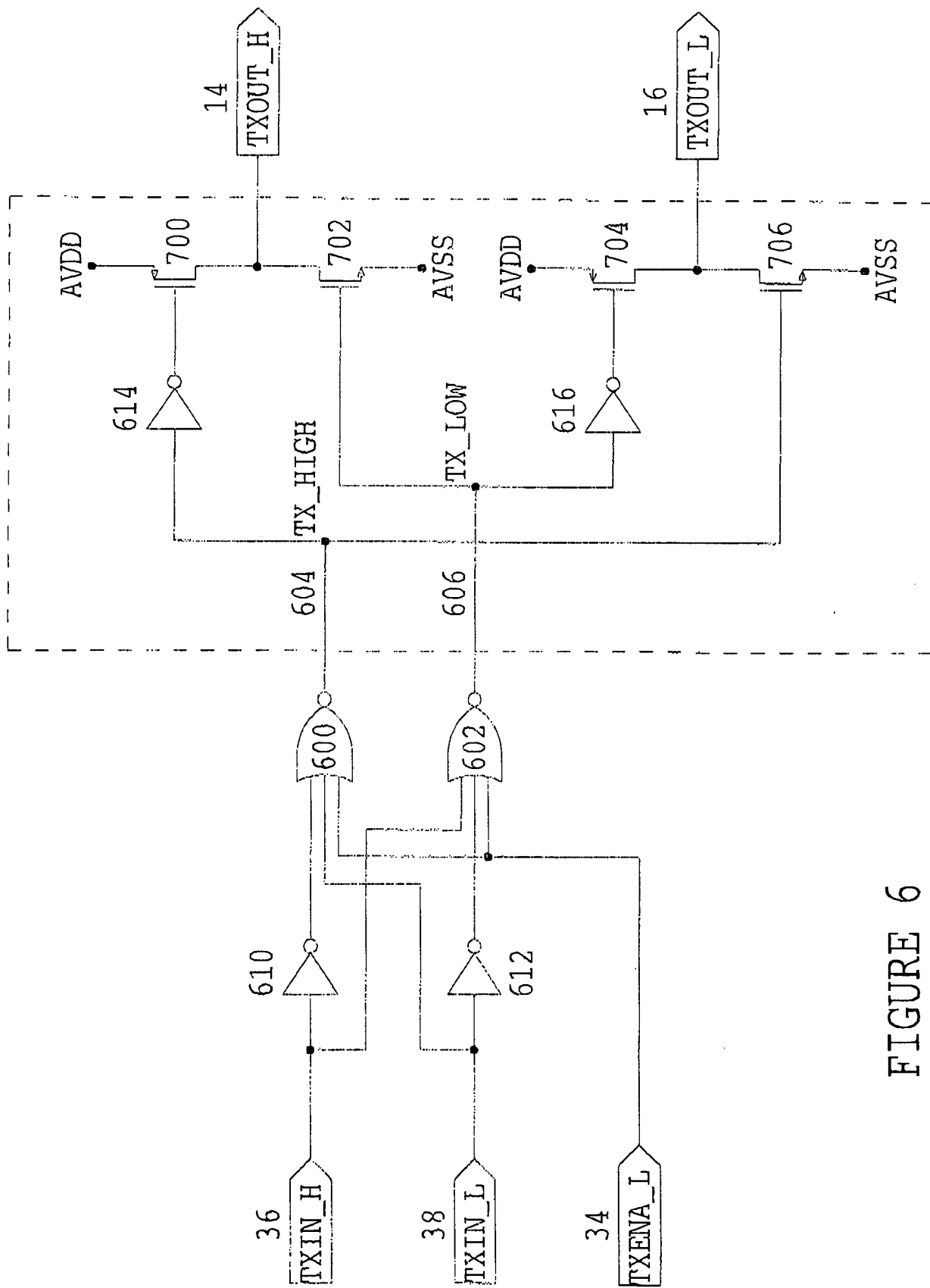


FIGURE 6

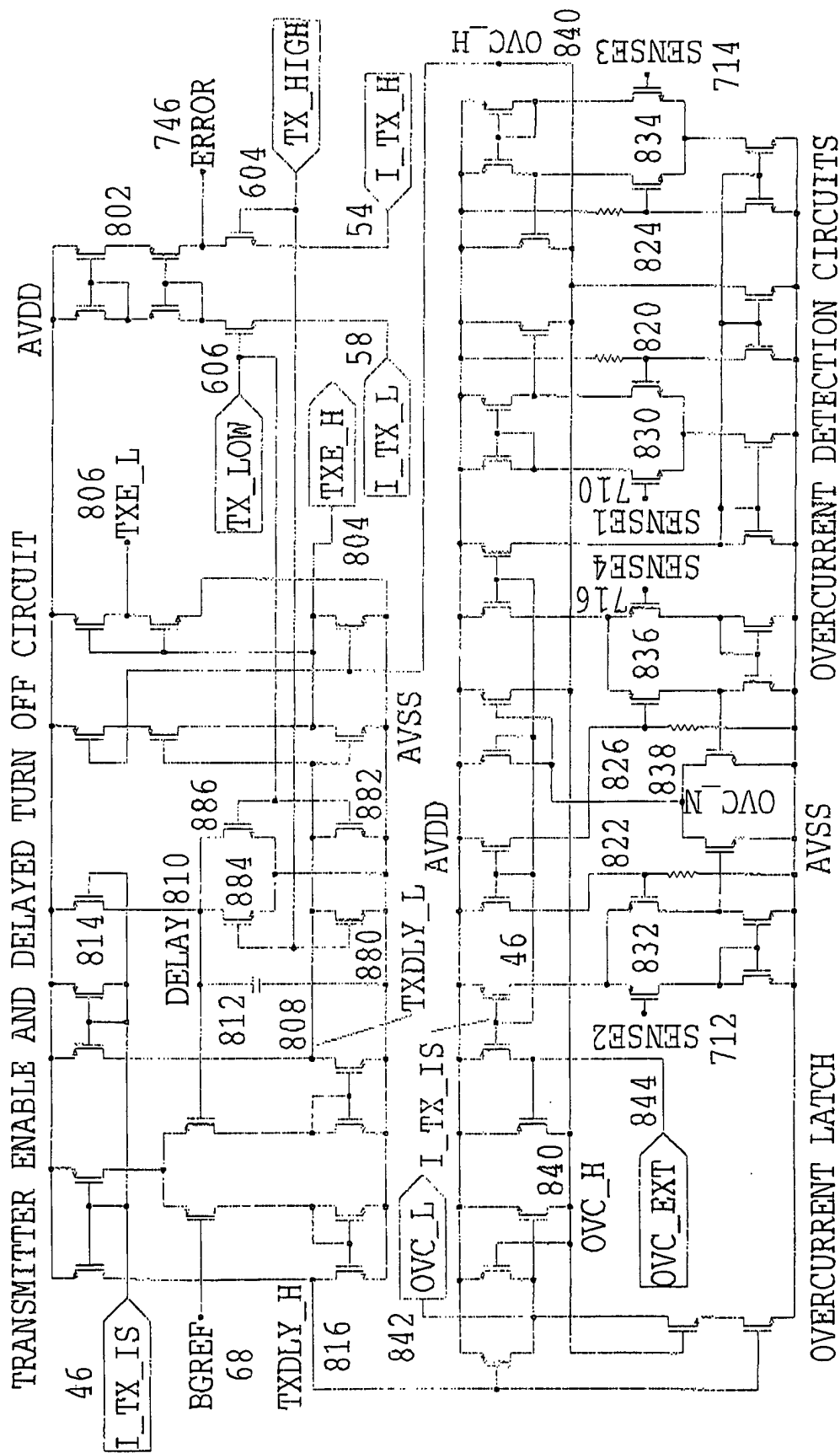


FIGURE 8

FIG. 9 is a block diagram of a system for transmitting and receiving data over a bus.

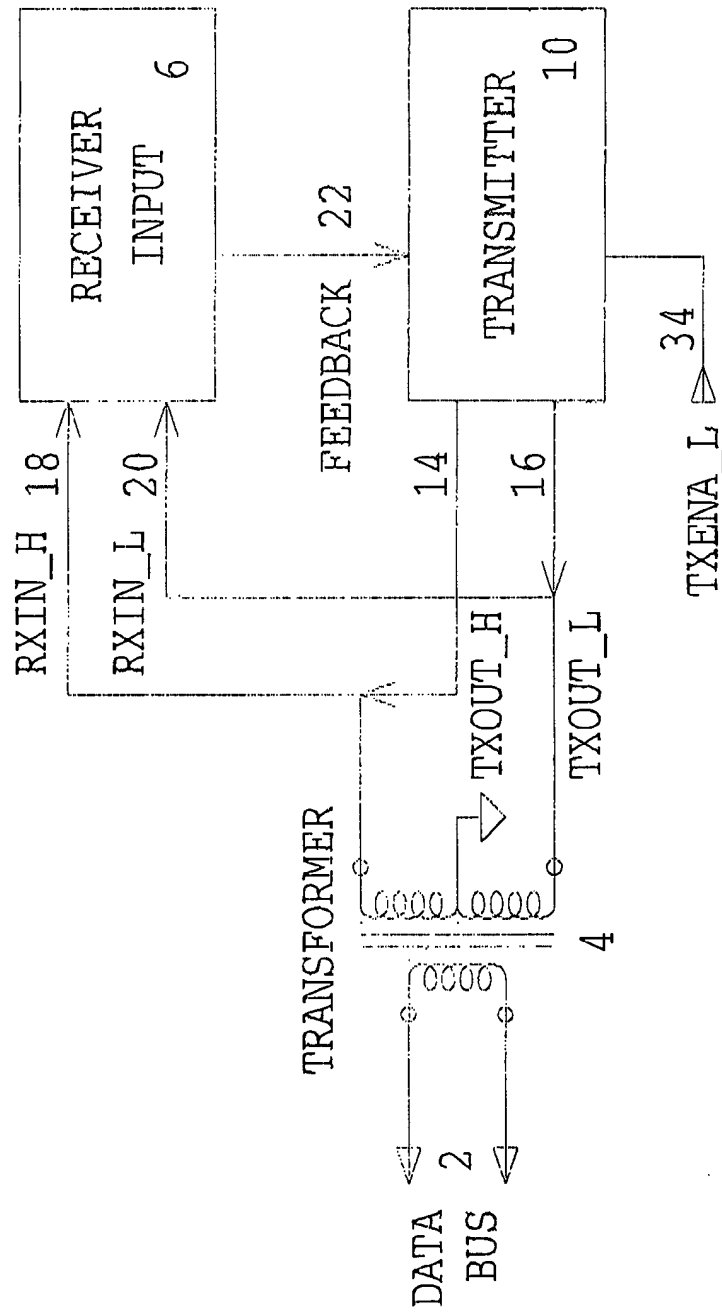


FIGURE 9

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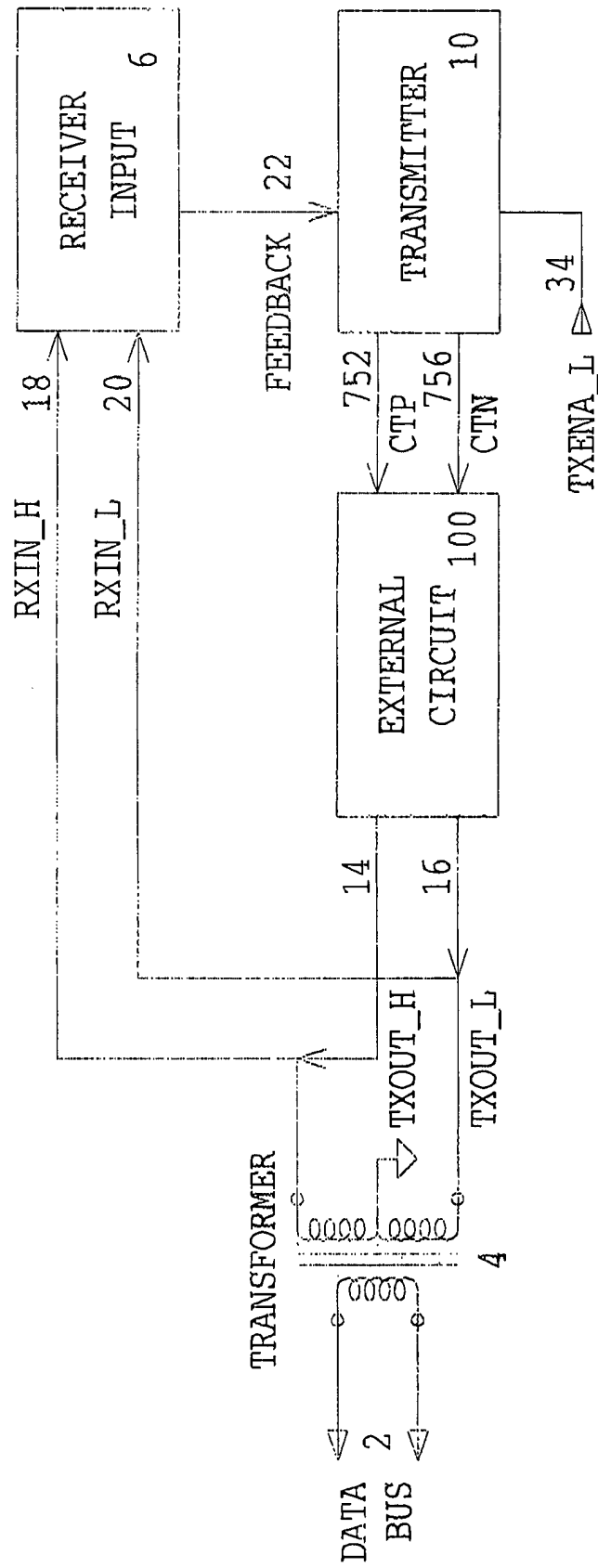


FIGURE 10

FIG. 11 is a schematic diagram of a circuit for generating a differential output signal. The circuit includes a differential pair of transistors 1102 and 1104, a tail resistor 1110, and a load resistor 1106. The gates of the transistors are driven by a common-mode input signal CTN (756) and a differential-mode input signal CTP (752). The gates are also biased by a tail current source 1102. The drains of the transistors are connected to a common-mode output signal TXOUT_H (14) and a differential-mode output signal TXOUT_L (16). The circuit is powered by a supply voltage VEE and a tail current source 1102.

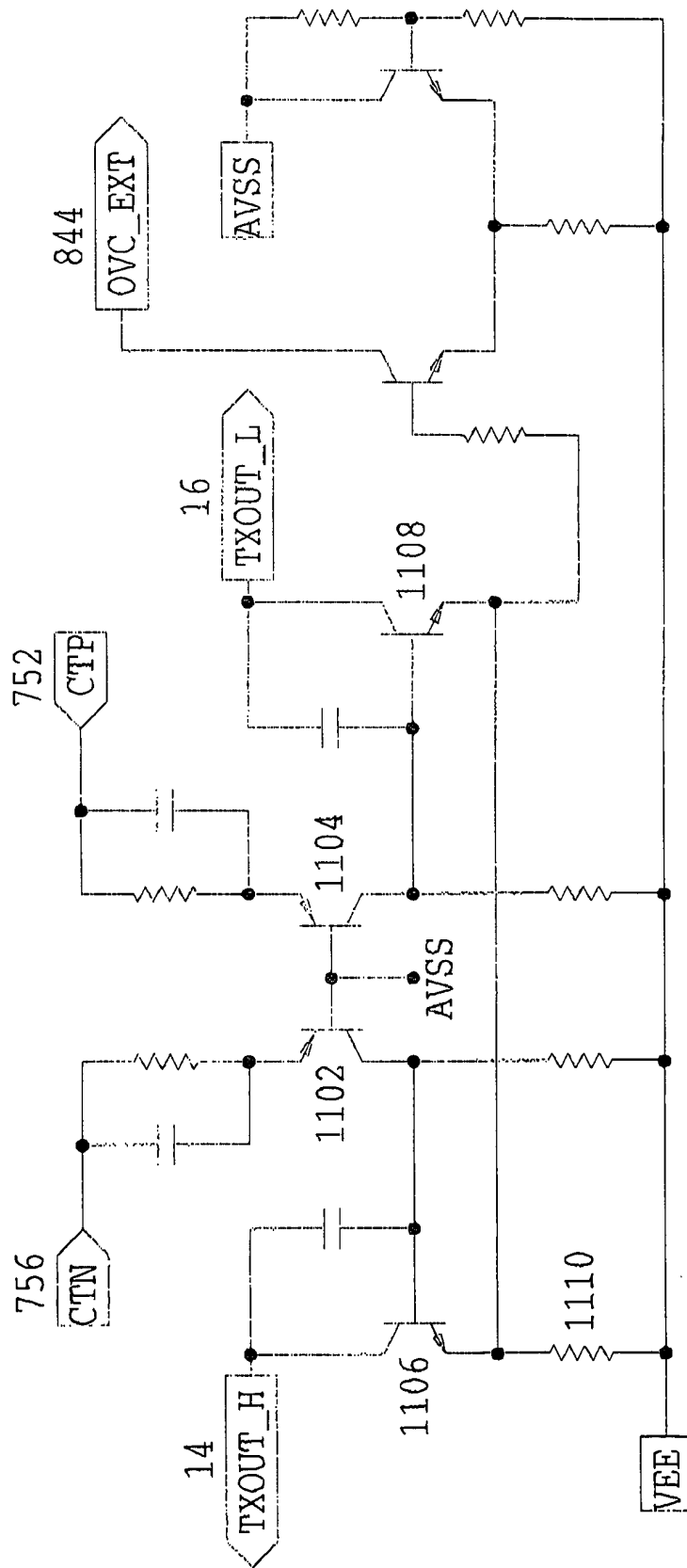


FIGURE 11

FIGURE 12

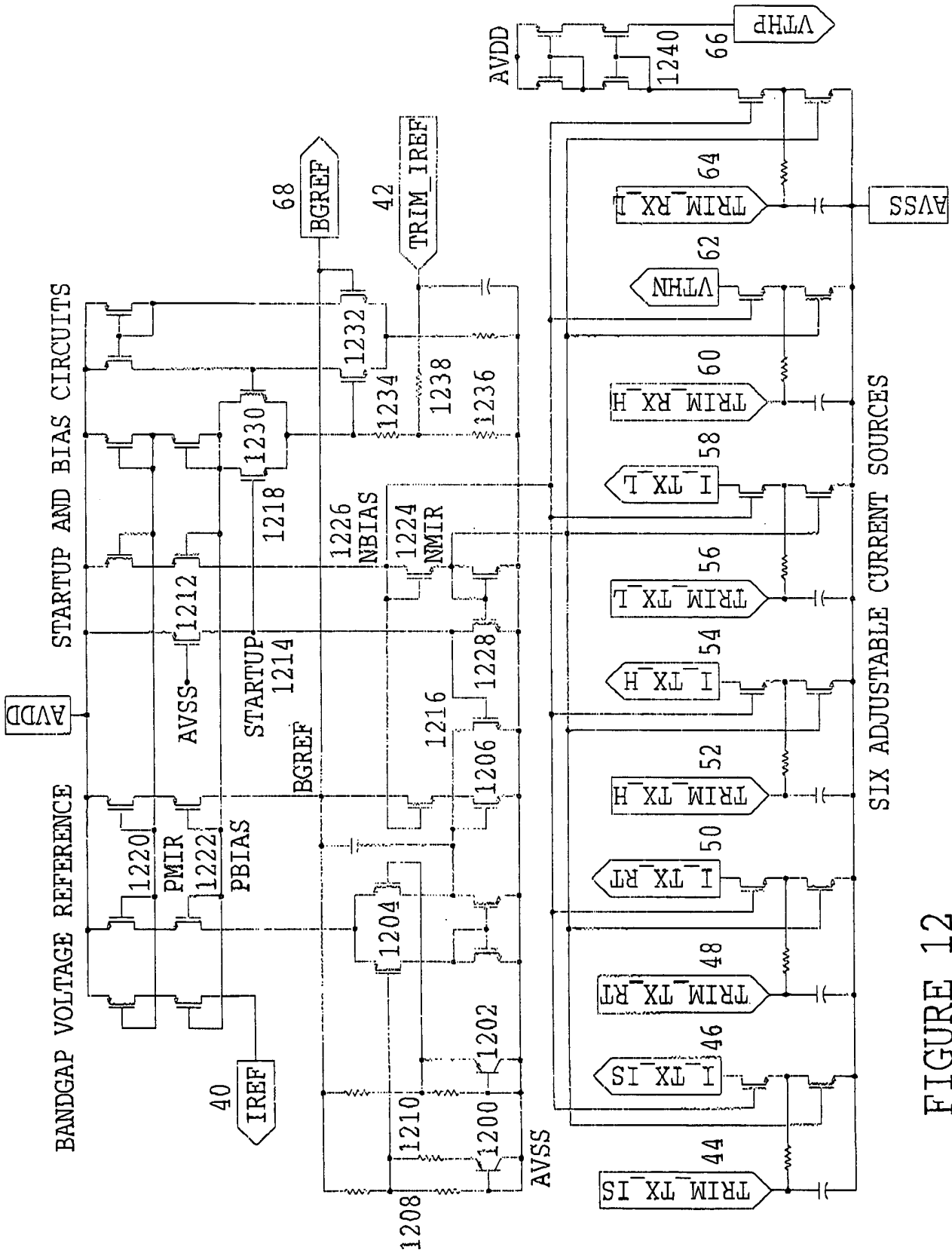


FIGURE 12